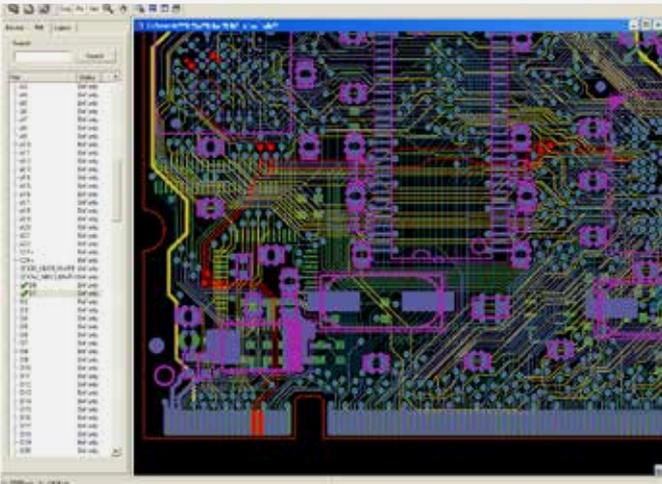


VISUALIZER - GRAPHICAL VIEWING TOOLS

Display fault reports on circuit schematics and layouts



Visualizer Highlights

- Schematic and board layout views with flexible highlighting of nets and components
- Support for hierarchical drawings
- User-configurable viewing screens
- Graphical support of design-for-test (DFT), fault-coverage activity
- Flexible color assignment to simplify boundary-scan analysis and fault class recognition
- Precise graphical representation support of diagnostic results produced by JTAG Technologies' test execution tools
- Directly linked to JTAG Technologies' ProVision application development environment
- Active-X version included for run-time test integration

Introduction

JTAG Visualizer is a design data viewer that integrates with the JTAG Technologies family of boundary-scan products. JTAG Visualizer accepts input data (schematic, layout, and information files) from a variety of sources to assist the user in understanding and acting upon the boundary-scan application. JTAG Visualizer's features fall into two functional groups, Graphical Representation and Exploration.

Applications

JTAG Visualizer adds to the power of boundary-scan throughout board design and manufacturing repair. Locating specific nets, components and other items in the schematics or layouts become simple and straightforward, even for the most complicated boards. For example, a designer may wish to check schematics and/or layouts for (boundary-scan) testability while repair technicians will benefit from faster graphical location of diagnosed faults.

Design and Test Engineering

In design, an important task is to assure 'testability', a process often referred to as Design-for-Test, or DFT.

Order Information

- JTVB - JTAG Visualizer for Board Layout - includes one CAD extractor/converter
- JTVS - JTAG Visualizer for Schematics - includes one CAD extractor/converter

Prerequisites

Software

- ProVision V2.0 or PSA or PIP/***. BSD Diagnostics recommended with layout viewer

Specifications Brief

Supported Schematic Systems

- Cadence - OrCAD Capture
- Mentor - CAMCAD, DxDesigner (EE 7.9.3 + and ViewDraw), Design Capture 2002/2004, PadsLogic 2005
- Zuken - CR5000, CadStar

Supported Layout Systems

- Valor ODB++
- Altium P-CAD
- Fabmaster FATF
- Mentor - PADS PowerPCB, BoardStation, Expedition, CAMCAD
- DDE-EDA - Supermax ECAD
- Intercept - Pantheon

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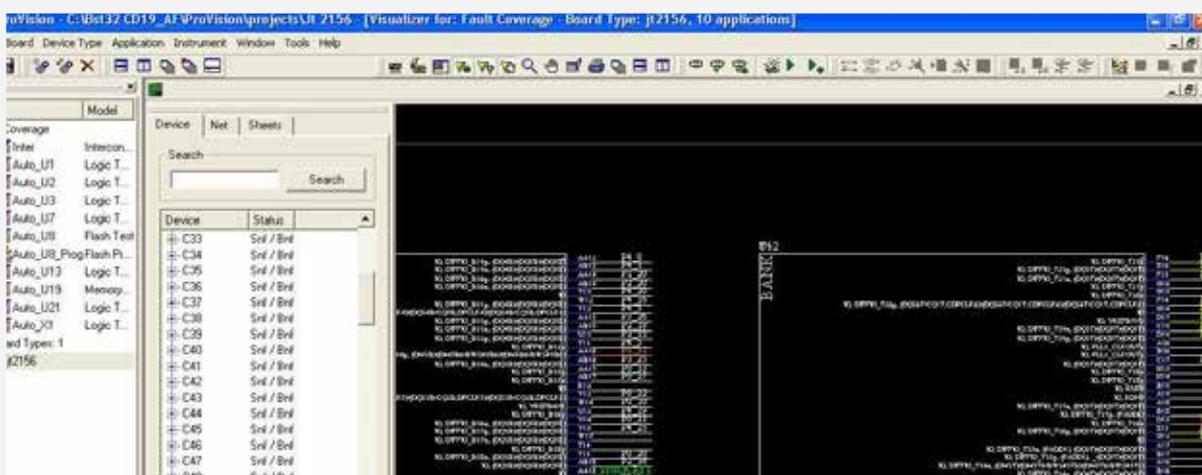
Boundary-scan's effectiveness is greatly enhanced by a formal approach to DFT prior to committing the design to layout. With JTAG Visualizer, designers can easily view the portions of the schematic defined as testable and which parts need improvement. This is achieved by combining the schematic data with test program data generated by JTAG Technologies' ProVision. Using customizable colors, test coverage can be represented in a color-coded schematic. Once the design has been optimized for boundary-scan test and committed to layout, final application development can begin in the JTAG ProVision. Direct links between ProVision's NetExplorer and JTAG Visualizer

allow the test developer to view constraints and potential conflicts in the schematic, allowing rapid circuit analysis.

Manufacturing

JTAG Visualizer greatly facilitates the repair of defective boards by showing the faults graphically in the layout and in the schematics. In this application JTAG Visualizer uses the diagnostic results file generated following test execution. By simply clicking on the net name or pin number in the diagnostic report, a technician can find all instances of the faulty net(s) within the physical layout or schematic circuit.

Figure 2



Visualizer Schematic Fault Coverage View

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