# RTG4 FPGAs

## Features and Benefits

### Radiation Tolerance

- Configuration Memory Upsets Immunity to LET > 110 MeV.cm$^2$/mg
- Single-Event Latch-up (SEL) Immunity to LET > 110 MeV.cm$^2$/mg
- SEU-Hardened Registers Eliminate the need for Triple-Module Redundancy (TMR)
  - Immune to Single-Event Upsets (SEU) to LET > 37 MeV.cm$^2$/mg
  - SEU Rate < $10^{-10}$ Errors/Bit-Day (GEO Solar Min)
- SRAM has built-in Error Detection and Correction (EDAC)
  - Upset Rate < $10^{-10}$ Errors/Bit-Day (GEO Solar Min)
  - Single-Bit Correction, Double-Bit Detection (SECDED)
- Single-event transient (SET) Upset Rate < $10^{-8}$ Errors/Bit-Day (GEO Solar Min) with Optional SET Filter
- Total Ionizing Dose (TID) > 100 Krad

### High-Performance FPGA

- Efficient 4-Input Lookup Tables (LUTs) with Carry Chains for High System Performance up to 300 MHz without SET Filter
- Up to 209 blocks of Dual-Port 24.5 kbit SRAM (Large SRAM) with 300 MHz Synchronous Performance (512 x 36, 1 kbit x 18, 2 kbit x 9, 2 kbit x 12)
- Up to 462 DSP Mathblocks with 18-bit x 18-bit Input Signed Multiplication and 44-bit Output Accumulator
  - High-Performance, 300 MHz (Without SET Filter) Across Military Temperature: -55C to 125C
- 16 SpaceWire Clock and Data Recovery Circuitry Instances, allowing High-Performance SpaceWire interface up to 400 Mbit/sec.
  Note: The SpaceWire Interface Protocol is not Included but can be implemented in the FPGA Fabric.

### High-Speed Serial Interfaces

24 Lanes of 3.125 Gbps Serialization/Deserialization (SERDES) supporting:

- XGXS/XAUI Extension (To implement a 10 Gbps XGMII Ethernet PHY interface)
- Native SERDES interface facilitates implementation of Serial RapidIO in FPGA Fabric or an SGMII interface to a Soft Ethernet MAC
- PCI Express®(PCIe) Gen1 Hard IP Core
  - x1, x2, x4 Lane(s) PCI Express Core
  - Up to 2 Kbytes Maximum Payload Size
  - 64-/32-bit AXI/AHB Master and Slave interfaces to the Application Layer

### High-Speed Memory Interfaces

Two High-Speed DDR2/DDR3 Memory Controllers:

- Supports DDR2 and DDR3 at 333 MHz (667 Mbps), LPDDR at 266 MHz (533 Mbps)-Max Clock Rate
- EDAC Option with SECDED
- Supports x9, x12, x18 and x36 Bus Widths

### Specifications

- 1.2 V Nominal Core Voltage
- Single-Ended I/Os: LVCMOS 1.2 V to 3.3 V, LVTTL, PCI
- Voltage Reference I/Os with Performance at 600+ Mbps
  - SSTL2, SSTL18, SSTL15, HSTL18, HSTL15
- True LVDS (600+ Mbps) Differential Receiver and True Current-Mode Driver, with Built-in Termination
- Clock Sources Include High-Precision 50 MHz Embedded RC Oscillator
- Up to 8 Clock Conditioning Circuits (CCCs) with PLLs
  - Frequency: Input 1 to 200 MHz, Output 20 to 400 MHz

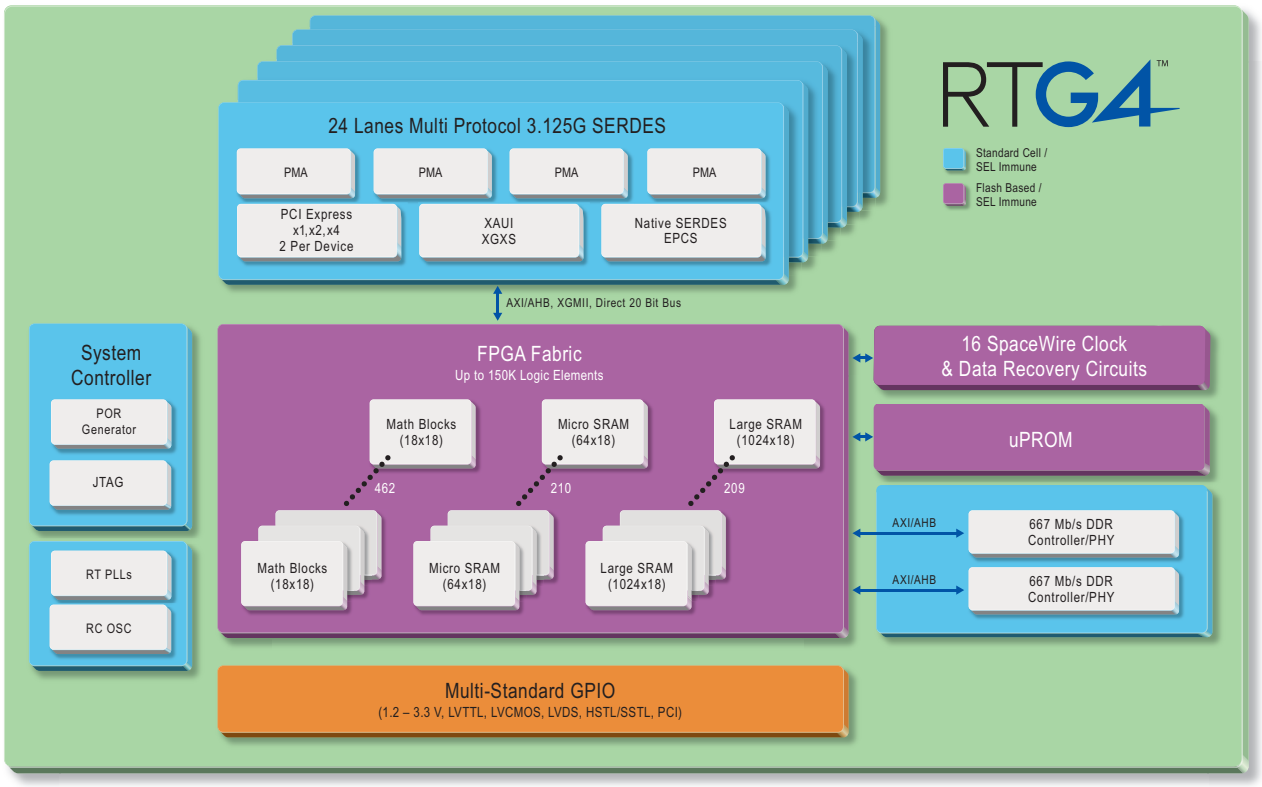
**Table 1 • RTG4 FPGA Product Family**

| Features | | RT4G150 |
|---|---|---|
| Logic/ DSP | Maximum Logic Elements (LUT4 + TMR flip-flop)* | 151,824 |
| | Mathblocks(18-bit x 18-bit) | 462 |
| | Radiation-Tolerant PLLs | 8 |
| Memory | LSRAM 24.5 kbit blocks | 209 |
| | uSRAM 1.5 kbit blocks | 210 |
| | Total SRAM Mbits | 5.3 |
| | uPROM kbits | 374 |
| High-Speed Interface | SERDES Lanes | 24 |
| | PCIe Endpoints | 2 |
| | DDR SDRAM Controllers (With ECC) | 2x32+4 bits ECC |
| | SpaceWire Clock and Data Recovery Circuits | 16 |
| User I/Os | MSIO (3.3 V) | 240 |
| | MSIOD (2.5 V) | 300 |
| | DDRIO (2.5 V) | 180 |
| | Total User I/Os (Non-SERDES) | 720 |

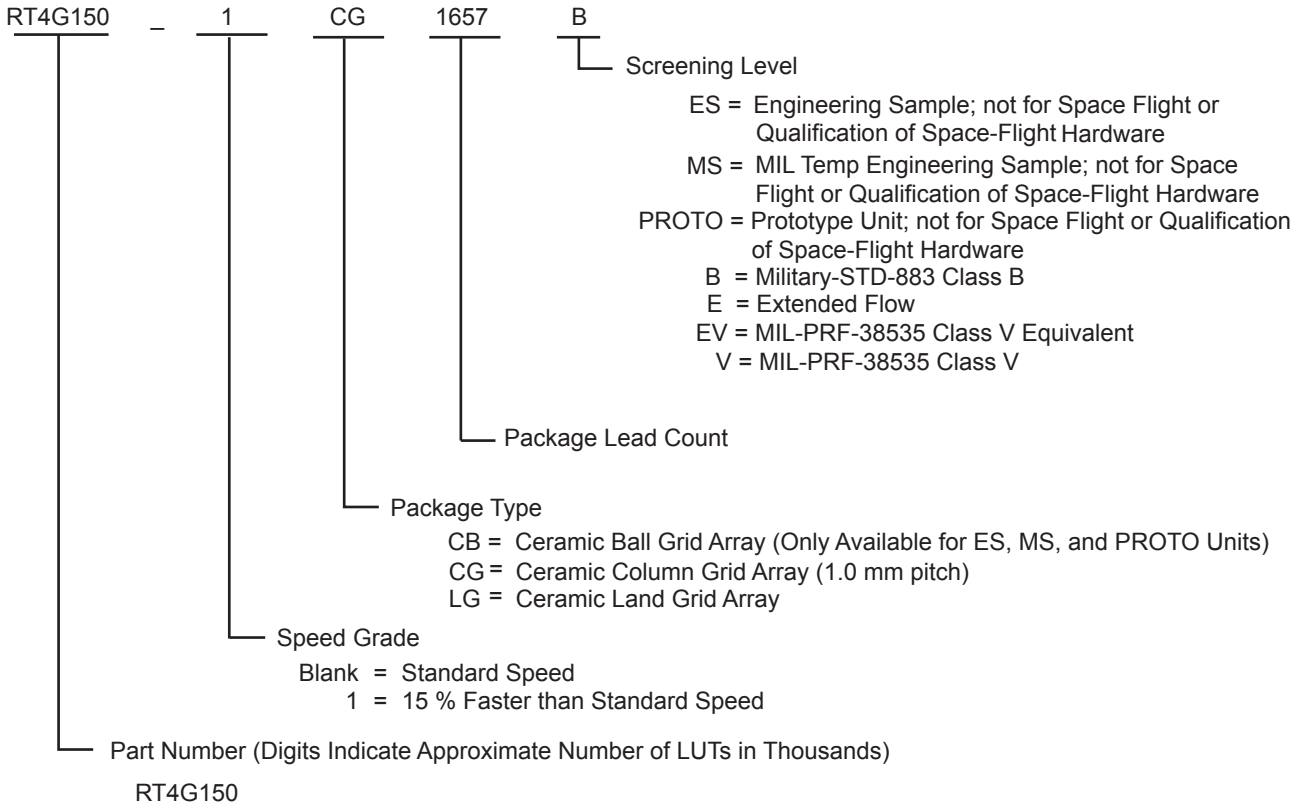
**Table 1 • RTG4 FPGA Product Family (continued)**

| Features | | RT4G150 |
|---|---|---|
| | Packages | CCGA/CLGA1657 |
| *Note: *Total Logic may vary based on utilization of DSP and memories in your design.* | | |

# RTG4 Device Block Diagram



# RTG4 Ordering Information




Contact your local *Microsemi SoC Products Group* representative for device availability. Refer to the *DS0131: RTG4 FPGA Datasheet* for device status.

# 1 – RTG4 Device Family Overview

RTG4 FPGAs integrate Microsemi's fourth-generation flash-based FPGA fabric and high-performance interfaces such as SERDES on a single chip while maintaining the resistance to radiation-induced configuration upsets in the harshest radiation environments, such as space flight (LEO, MEO, GEO, HEO, deep space); high altitude aviation, medical electronics, and nuclear power plant control. The RTG4 family offers up to 151,824 registers, which are hardened by design against radiation-induced SEUs. Each RTG4 logic element includes a LUT4 with fast carry chains providing high-performance FPGA fabric up to 300 MHz. There are multiple embedded memory options and embedded multiply-accumulate blocks for digital signal processing (DSP) up to 300 MHz. A high-speed serial interface provides 3.125 Gbps native SERDES communication, while double data rate DDR2/DDR3/LPDDR memory controllers provide high- speed memory interfaces.

## High-Performance FPGA Fabric

Built on 65 nm process technology, the RTG4 FPGA fabric is composed of four building blocks: the logic module, LSRAM, uSRAM, and mathblocks. The logic module is the basic logic element and has these advanced features:

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate SEU-hardened flip-flop that can be used independently from the LUT. Each flip-flop has its own synchronous reset while there is only one global asynchronous reset that drives all flip-flops.

The 4-input LUTs can be configured either to implement a 4-input combinatorial function or to implement an arithmetic function, where the LUT output is XORed with the carry input to generate the sum output.

### Dual-Port LSRAM

The LSRAM block is targeted for storing large amounts of data for use with various operations. Each LSRAM block can store up to 24,576 bits. It contains two independent data ports: Port A and Port B. The LSRAM block is synchronous for both Read and Write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

### Three-Port uSRAM

The uSRAM block is the second type of SRAM block that is embedded in the fabric of the RTG4 devices. The uSRAM block is a 3-port SRAM; it has two read ports (Port A and Port B) and one write port (Port C). The two read ports are independent of each other and can perform Read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block can store up to 1,536 bits. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric master. The uSRAM block can also be used to store DSP coefficients.

### uPROM Non-Volatile Memory

uPROM is a non-volatile flash memory, which uses the same flash technology as the FPGA configuration cells. uPROM is immune to memory upsets and has a TID performance beyond 100 krad, similar to the FPGA flash configuration cells. The RTG4 devices have up to 374 kbits of uPROM memory. The uPROM can be used for power-on initialization of RAMs and embedded IPs, as well as storage for DSP coefficients. The uPROM has a read performance of 50 MHz.

### Mathblocks for DSP Applications

The fundamental building block in any DSP algorithm is the multiply-accumulate function. The RTG4 FPGA device implements a custom 18-bit x18-bit Multiply-Accumulate (18x18 MACC) block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18x18 signed multiplications natively (A[17:0] x B[17:0])
- Supports dot product; the multiplier computes: (A[8:0] x B[17:9] + A[17:9] x B[8:0]) x $2^9$
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. RTG4 uSRAMs are ideally suited to serve the needs of coefficient storage while the LSRAMs are used for data storage.

## High-Speed Serial Interfaces

### SERDES Interface

RTG4 has up to six 3.125 Gbps Quad SERDES transceivers, each supporting the following:

- 4 SERDES/EPCS lanes (24 total SERDES lanes)
- The native SERDES interface facilitates implementation of serial rapidIO (SRIO) in fabric or a 10 Gigabit Media Independent Interface (SGMII) for a soft Ethernet MAC.

### PCI Express (PCIe)

PCIe is a high-speed, packet-based, point-to-point, low pin count, serial interconnect bus. The RTG4 family has embedded high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block and following are the main features supported:

- Supports x1, x2, and x4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0 (at Gen1 rate of 2.5 Gbps only)
- 2.5 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 kbytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)

### XAUI/XGXS Extension

The XAUI/XGXS extension utilizes four SERDES channels operating at 3.125 Gbps to allow the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

# High-Speed Memory Interfaces: DDR2/3 Memory Controllers

There are up to two fabric DDR (FDDR) subsystems present in the RTG4 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. Each FDDR block provides an interface to/from the FPGA fabric.

The following are the main features supported by the FDDR blocks:

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance for DDR2 and DDR3
- Up to 533 Mbps (266 MHz double data rate) performance for LPDDR
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM bus width modes: x8, x16, and x32 (or x9, x18, and x36 with SECDED enabled)
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

Each FDDR subsystem has an interface to the DDR memories. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by a master in the FPGA fabric.

# Clock Sources: On-Chip Oscillators, PLLs, and CCCs

RTG4 devices have an on-chip 50 MHz RC oscillator, which is available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. The oscillator can be used in conjunction with the integrated user phase-locked loops (PLLs) and CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, this oscillator is also used by the system controller and power-on-reset circuitry.

RTG4 devices have up to eight fabric CCC blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. Each of the PLL and oscillator clock sources are radiation-hardened to provide glitchfree clocks in the system. The user can use any of the eight PLLs and CCCs to generate the fabric clocks from the base fabric clock (CLK_BASE).

# Radiation and Reliability

RTG4 FPGAs are manufactured on a low-power 65 nm process with substantial reliability heritage. RTG4 FPGAs will be qualified to MIL-STD-883 Class B, and Microsemi will seek QML Class Q and Class V qualification.

RTG4 FPGAs are immune to radiation-induced (SEU-induced) changes in configuration, due to the robustness of the flash cells used to connect and configure logic resources and routing tracks.

No background scrubbing or reconfiguration of the FPGA is required to mitigate changes in configuration due to radiation effects. Data errors, due to radiation, are mitigated by hardwired SEU-resistant flip-flops in the logic cells and in the mathblocks. SSECDED protection is optional for the embedded SRAM (LSRAM and uSRAM) and the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one-bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories.

# RTG4 Development Tools

## Design Software

Microsemi's Libero® System-on-Chip (SoC) software is a comprehensive software toolset to design applications using the RTG4 device. The Libero SoC software manages the entire design flow from design entry, synthesis and simulation, place-and-route, timing and power analysis, with enhanced integration of the embedded design flow. System designers can leverage the easy-to-use Libero SoC that includes the following features:

- Synthesis, DSP, and debug support from Synopsys®
- Simulation from Mentor Graphics®
- Push-button design flow with power analysis and timing analysis
- SmartDebug for access to non-invasive probes within the RTG4 devices

For more information refer to *Libero SoC.*

## Design Hardware

Microsemi’s RTG4 Development Kit provides designers with an evaluation and development platform for applications such as: data transmission, serial connectivity, bus interface, and high-speed designs using the RTG4 devices. The development board features an RT4G150 device offering 151,824 logic elements in a ceramic package with 1,657 pins.

The RTG4 development board includes two 1 GB DDR3 and 2 GB of SPI flash memories. The board also has several standard and advanced peripherals such as: PCIe x4 edge connector, two FMC connectors for using several off-the-shelf daughter cards, USB, Philips
inter-integrated circuit (I2C), gigabit Ethernet port, serial peripheral interface (SPI), and UART. A high precision operational amplifier circuitry on the board helps to measure the core power consumption by the device. There is a FlashPro programmer embedded on the board allowing programming of the RTG4 FPGA through the JTAG interface. For more information refer to *Dev Kits and Boards.*

## IP Cores

Microsemi offers many soft peripherals that can be placed in the FPGA fabric of the device. These include Core1553, CoreJESD204BRX/TX, CoreFIR, CoreFFT, and many other DirectCores. Refer to *IP Cores* for more information.

# 2 – Product Brief Information

## List of Changes

The following table lists critical changes that were made in each revision of RTG4 Product Brief.

| Revision | Changes | Pages |
|---|---|---|
| Revision 1.6 (September 2015) | Removed reference to RT4G075 device (SAR 70694). | N/A |
| | Table 1 was updated for uPROM kbits (SAR 66983). | 1-I |
| | "Specifications" section updated for LVDS I/O standards information (SAR 69465). | 1-I |
| | "RTG4 Device Block Diagram" were updated (SAR 70694). | 1-II |
| Revision 1.5 (May 2015) | "RTG4 Device Block Diagram" and "uPROM Non-Volatile Memory" section were updated (SAR 66992). | 1-II, 1-1 |
| Revision 1.4 (April 2015) | Removed all references to the RT4G200 device and the CG/LG2092 package, Added User I/Os break-down information to Table 1. Added software, hardware and IP information to the "RTG4 Development Tools" section. Removed the Device Status table (Table 2) and replaced it with the *RTG4 FPGAs Datasheet* as a reference. Removed two references to the SII bus.(SAR 65824) | N/A, 1-I 1-4, 1-III |
| Revision 1.3 (November 2014) | Table 1 was updated (SAR 62641) and minor language edits were made. | 1-I |
| Revision 1.2 (August 2014) | Added TM symbol to RTG4 logo. | 1-I |
| Revision 1.1 (July 2014) | Clarified Military temp testing in "RTG4 Device Block Diagram" and space environments in the "RTG4 Device Family Overview" section. | 1-II, 1-1 |
| Revision 1 (May 2014) | "High-Performance FPGA" sections updated. Total SRAM information updated in Table 1. | 1-I,1-1 1-I |
| Revision 0 (December 2013) | Initial Release | N/A |

## Datasheet Categories

### *Categories*

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as referenced in the *UG0131: RTG4 FPGA Datasheet,* is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### *Product Brief*

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### *Advance*

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### *Preliminary*

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### *Production*

This version contains information that is considered to be final.

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